SEMICONDUCTOR ETCH SPEED MODIFICATION

Abstract of the Disclosure

In accordance with embodiments of the methods of the present invention, a sacrificial layer provides an etch speed modification to effectively etch multiple semiconductor devices having dissimilar materials to a common layer or substrate with a common etch process. The time to etch remove a second exposed portion is compared with the time to etch remove a first exposed portion, and a sacrificial layer is deposited on the first exposed portion having a time to etch remove substantially equal to the difference. The sacrificial layer is provided to have predetermined material composition, material property and layer thickness, among other things, to provide a desired time to etch remove. The methods also provide for self-aligned via formation providing highly defined vias by the etch removal of sacrificial material rather than direct etching of the vie. The methods also provide planarization between two or more devices.